4) Set R519 for the required I.D. time interval. This adjustment can be made by keeping the repeater COR circuits active, (with an R.F. signal or open squelch) and noting the time interval between I.D.'s. A faster method of adjustment is possible if an oscilloscope with an accurately calibrated time base is available. Connect the scope probe to pin 10 or 11 of U508 and note the pulse stream which is generated when the COR circuits are active. Calculate the required pulse period from the formula T pulse = $\frac{\text{time (seconds).}}{8192}$ The result of this calculation is the required time pulse to pulse. (e.g., For 10 minutes (600 seconds), T pulse = $\frac{600}{8192}$ = 73ms) Set R519 for the required T pulse period. (13.6Hz for 10 min. with a Counter.)

5) If the local Mic Amp is used, set the level pot for the desired Mic Gain.

ID250A ID/AUDIO AMP. & MIXER BOARD

THEORY OF OPERATION

NOTE: Unless otherwise noted, in the following discussion any reference to a "high" logic state shall be defined as a voltage of at least 70% of the positive power supply voltage (3.5 volts in the case of a 5 volt supply), and a "low" logic state shall be a voltage of no more than 20% of the positive supply (1 volt in the case of a 5 volt supply). These levels will typically be full positive supply (+5V) and zero volts respectively.

Referring to the schematic diagram, notice that two trigger inputs are provided at E512 and E513, either one of which can be used, depending on the sense of the input source. Assuming that neither trigger input has been activated for some time, pin 10 of U504 will remain low, and transistor Q503 will be held in the off state, allowing C511 to charge through R529. If the trigger inputs remain inactive long enough (approximately 1½ minutes), C511 will charge up to the threshold point of the U508 flip-flop, causing pin 4 of U508 to go high and pin 3 of U508 to go low. The high state on pin 4 causes the I.D. timer clock to stop (via the high state on pin 8 of U508), and simultaneously resets the I.D. clock counter, U509, to its zero state. The unit is now in the standby condition, and will be activated immediately upon the next trigger input.

When a trigger signal arrives, it will cause pin 10 of U504 to go high, which in turn, causes the U508 flip-flop to be set, and also causes Q503 to keep C511 discharged as long as there is input activity at intervals of less than 1½ minutes. As soon as the U508 flip-flop is set, the high level on pin 3 is converted by C502 and R513 into a short positive going spike which passes through D511 and sets the trigger flip-flop, U505, causing an I.D. to be generated immediately. (Details of the I.D. generation sequence will follow later.) As long as the activity timer detects input activity, pin 4 of U508 will remain low and the U508 I.D. clock will be allowed to run, producing positive pulses at its 13 hertz (nominal) rate. These pulses trigger U509, a binary divider which divides the 13 hertz clock by 8192. Thus, as long as the I.D. clock is running, the output of U509 (pin 3) will go high about every 600 seconds (approximately 10 minutes), and will trigger the U505 flip-flop, causing an I.D. sequence to be generated. Note that the output pulse on pin 3 of U509 is also routed, via diode D513, back to the U509 reset input, resetting the divider to its zero state, and allowing another timing cycle to start.