# SPECTRUM COMMUNICATIONS

## CTC100
## Theory of Operation

Referring to the schematic, a DC voltage proportional to receiver "background" noise is taken from the wiper of the "SQUELCH" control and applied to pin 23 of the COR board. This voltage is amplified and conditioned by COR amplifiers Q7 and Q6 and applied to one input of NOR gate U2D. The output of Q6, available at pin 24, is a level shifted and filtered voltage which is used to activate the receiver audio stages coincidentally with the activation of the COR. The remaining input of U2D is driven from the output of U3A, a flip-flop which is toggled by the front panel "COR SIMULATE" pushbutton. The output of U3A also drives Q5, the "COR SIMULATE" indicator lamp driver. The output of U2D then, is a logic "high" in the presence of either a simulated or an actual signal acquisition, and is used to drive Q3, the "INCOMING SIGNAL" indicator lamp driver. This logic level is switched by the front panel "COR DISABLE" switch and is used to trigger the "HANG" timer which consists of Q1, and NOR gates U1A and U1B.

The "HANG" timer works in the following manner: A "COR" activation causes pin 9 of U1B to go "high" which in turn causes the U1A-U1B flip-flop to be set. Simultaneously, transistor Q1 is turned on, causing the 10uF capacitor to rapidly discharge. At this point pins 3 and 10 of U1 are at logic levels "one" and "zero" respectively, and remain in this state as long as the COR is activated. Upon deactivation of the COR, pin 9 of U1B goes"low", and transistor Q1 turns off, allowing the 10uF capacitor to charge through R9, the front panel "HANG TIME" pot. When the 10uF capacitor has charged to the threshold point of U1A, the U1A-U1B flip-flop is reset and returns to the standby mode.

The "TIME-OUT" timer operates in the following manner: Upon activation of the COR, and for the duration of COR activation, pin 3 of U1 will be high, and pin 10 of U1, as well as pin 11 of U1, will be low. The low condition on pins 10 and 11 of U1 will cause transistor Q4 to be in the off state, and the high condition on pin 3 will cause the 220uF capacitor to charge through the front panel "TIME-OUT" pot. When the voltage on the 220uF capacitor reaches the threshold of U2A, pin 1 of U2B will go "low", triggering the U2B-U2C flip-flop. At this point the timer is in the "timed-out" state with pins 3 and 10 of U2 at logic "one" and "zero" respectively. The timer remains in this state until a negative transition appears at board terminal #5, at which time the U2B-U2C flip-flop will be reset. Depending on which jumper wire configuration is selected (term. #5 & 4, or term.#5 & 7) time-out reset will occur either upon COR deactivation (removal of RCVR signal) or upon "HANG" timer reset (transmitter drop).

The normally low output from the time-out timer and the active low output from the hang timer are summed in NOR gate U2D, which turns on the transmitter PTT driver, Q8. Also summed into U1D is the output of the reset inhibit flip-flop, U3B. Momentary activation of the "LOCAL INHIBIT/RESET" pushbutton will cause the control flip-flop to change state and either set or reset the transmitter inhibit condition. The inhibit condition is indicated by the activation of the inhibit lamp driver, Q9. A pair of inputs are provided for remote inhibit and reset through terminals 20 and 19 respectively.

A positive going pulse of Vcc amplitude on pin 20 will inhibit the transmitter, while a similar pulse on pin 19 will reset the unit to normal operation.